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Electronic Patent Application Submission

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EFS ID:	63386
Application ID:	10709920
Title of Invention:	Concurrent Processing Memory
First Named Inventor:	Chengpu Wang
Domestic/Foreign Application:	Domestic Application
Filing Date:	2004-06-05
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Attorney Docket Number:	NONE
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Expiration Date:	05312005
Card Holder Name:	Chengpu Wang
Postal Code:	11733
RAM Payment Status:	RAM success
RAM User ID:	EFSPROD
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Digital Certificate Holder: cn=Chengpu Wang,ou=Independent Inventors,ou=Patent and Trademark Office,ou=Department of Commerce,o=U.S. Government,c=US
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TRANSMITTAL

Electronic Version v1.1
Stylesheet Version v1.1.0

Title of Invention	Concurrent Processing Memory

Application Number: 10/709920
Date: 2004-06-05
First Named Applicant: Dr. Chengpu Wang

Confirmation Number: 3919
Attorney Docket Number:

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Submitted by:	Elec. Sign.	Sign. Capacity
Dr. Chengpu Wang	/CP/Wang	Inventor

Documents being submitted	Files
us-fee-sheet	InfoDisc-usfees.xml
	us-fee-sheet.xsl
	us-fee-sheet.dtd
us-ids	InfoDisc-usidst.xml
	us-ids.dtd
	us-ids.xsl

Comments

FEE TRANSMITTAL

Electronic Version v08
Stylesheet Version v08.0

Title of Invention	Concurrent Processing Memory

Application Number: 10/709920
Date: 2004-06-05
First Named Applicant: Dr. Chengpu Wang
Attorney Docket Number:

TOTAL FEE AUTHORIZED $180

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BASIC FILING FEE

Fee Description	Fee Code	Amount $	Fee Paid $
Submission Of Information Disclosure Stmt Fee	1806	180	180

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention	Concurrent Processing Memory

Application Number: 10/709920
Confirmation Number: 3919
First Named Applicant: Chengpu Wang
Attorney Docket Number:
Search string: (6460127 or 6404439 or 6711665 or 6275920 or 4215401 or 4739474 or 6073185 or 5809322 or 5717943 or 5710932 or 5546343 or 5421019 or 5134711 or 5095527 or 5038282 or 6049859 or 6173388 or 5752068 or 5729758 or 5590356 or 5555428 or 5418915 or 5175858 or 4992933 or 4775952 or 4380046).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6460127	2002-10-01	Apparatus and method for signal processing		712	14
	2	6404439	2002-06-11	SIMD control parallel processor with		712	14
	3	6711665	2004-03-23	Associative processor		712	14
	4	6275920	2001-08-14	Mesh connected computed		712	14
	5	4215401	1980-07-29	Cellular digital array processor		712	10
	6	4739474	1988-04-19	Geometric-arithmetic parallel processor		712	14
	7	6073185	2000-06-06	Parallel data processor		710	1
	8	5809322	1998-09-15	Apparatus and method for signal processing		712	14
	9	5717943	1998-02-10	Advanced parallel array processor (APAP)		712	14
	10	5710932	1998-01-20	Parallel computer comprised of processor elements		712	14
	11	5546343	1996-08-13	Method and apparatus for a SIMD on a memory chip		712	14

	12	5421019	1995-05-30	Parallel data processor	712	14
	13	5134711	1992-07-28	Computer with intelligent memory system	712	14
	14	5095527	1991-01-31	Array processor	712	14
	15	5038282	1991-08-06	Geometric-arithmetic parallel processor	712	14
	16	6049859	2000-04-11	Image-processing processor	712	17
	17	6173388	2001-01-09	Directly accessing local memories of array	712	22
	18	5752068	1998-05-12	Mesh parallel computer architecture apparatus and	712	16
	19	5729758	1998-03-11	SIMD processor operating with a plurality of	712	22
	20	5590356	1996-12-31	Mesh parallel computer architecture	712	31
	21	5555428	1996-09-10	Activity masking with mask context of SIMD	712	16
	22	5418915	1995-05-23	Arithmetic unit for SIMD type parallel computer	712	22
	23	5175858	1992-12-29	Mechanism providing concurrent	712	22
	24	4992933	1991-02-12	SIMD array processor with global instruction	712	22
	25	4775952	1988-10-04	Parallel processing system apparatus	712	22
	26	4380046	1979-05-12	Massively parallel processor computer	712	22

Remarks

Note: Remarks are not for responding to an office action.

The topic of this utility patent application has been presented as: (1) An conference application to PDPTA 2003, on 2003/04/22, via email, to Hamid Arabnia [hra@cs.uga.edu]. (2) An conference application to PPoPP 2003, on 2003/04/22, via email, to Martin Rinard [rinard@cag.lcs.mit.edu]. (3) A paper submission to Parallel Computing, on 2003/05/02, via email, to Daniel A. Reed [Dan_Reed@unc.edu]. The paper entered the full reviewing proccess by a review board for a year before finally rejected. (4) An conference presentation at PDPTA 2003, on 2003/06/23, at 04:50-05:10pm, as "A Smart Memory Concept". (5) An invited talk at Brookhaven National Lab, on 2003/07/23, at 2:00-3:00pm, as "A Smart Memory Design". (6) A full length paper in the conference proceeding of PDPTA 2003, at page 1926-1932, editted by Hamid Arabnia [hra@cs.uga.edu]. The conference paper was sent to a few people who showed interest directly. (7) A grant application by Prof. Sangjin Hong [snjhong@ece.sunysb.edu]. (8) A regular paper submission to IEEE Transactions on Computers [tc@computer.org]. The Reference list for the paper submission is: [1] E. R. Davies, Machine Vision: Theory, Algorithms, Practicalities (Academic Press, 1990). [2] T. J. Fountain, Parallel Computing: Principle and Practice (Cambridge, 1994); [3] John

P Hayes, Computer Architecture (McGraw-Hill, 1988). [4] John L. Hennessy, David A. Patterson, Computer Organization and Design (Morgan Kaufmann 1998); [5] M. Hall, P. Kogge, J. Koller, P. Diniz, J. Chame, J. Draper, J. LaCoss, J. Granacki, J. Brockman, A. Srivastava, W. Athas, V. Freeh, J. Shin, and J. Park. Mapping Irregular Applications to DIVA, a PIM-Based Data-Intensive Architecture. In: Supercomputing, November 1999. [6] Y. Kang, W. Huang, S. Yoo, D. Keen, Z. Ge, V. Lam, P. Pattnaik, and J. Torrellas. Flexconventional random access memory: Toward an Advanced Intelligent Memory System. In: International Conference on Computer Design, pages 192-201, October 1999. [7] M. Oskin, F. Chong, and T. Sherwood. Active Pages: A Computation Model for Intelligent Memory. In: International Symposium on Computer Architecture, pages 192-203, June 1998. [8] K. Mai, T. Paaske, N. Jayasena, R. Ho, W. Dally, M. Horowitz. Smart Memories: A Modular Reconfigurable Architecture. In: ISCA, June 2000. [9] R. J. Offen, VISL Image Processing (McGraw-Hill, 1986). [10] C. P. Wang, and Z. Wang, A Smart Memory Design. In: Parallel and Distributive Processing, Technology, and Application, June, 2003.

Signature

Examiner Name	Date